REMARKS

AMENDMENT TO THE DRAWINGS

It is asserted in the Office Action that Figures 1-4 are objected to because the drawings are not formal. Applicant also notes the assertion the Office Action that the drawings are acceptable for examination purposes. Applicant, however, submits formal drawings for which approval is respectfully requested.

Claims 1-20 were examined and reported in the Office Action. Claims 1-20 are rejected. Claims 1, 6, 10, and 18-19 are amended. Claims 1-20 remain. Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 112, Second Paragraph

It is asserted in the Office Action that claims 1-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. Applicant respectfully disagrees.

Applicant's specification agrees with the claim language in that on page 10, line 24 to page 11, line 3, Applicant defines $n = a + \log_2 i$, where $\log_2 i$ = number of instruction bits, Applicant gives an example where i can be found (*i.e.*, where the number of instruction bits equals 8, i = 256). Further, on page 11, line 20 to page 12, line 5, Applicant defines another embodiment, In this embodiment, Applicant defines five components (i)-(v). Clearly component "(i)" and the "i" in the number of bits equation are distinguishable. Further, as Applicant explains in the specification (*id.*), component "(i)", which represents instruction register contents (8 bits), is not represented as the "i" in the number of instruction bits equation, as it is clear on line 5 that $\log_2 256$ is component "(i)." And, Applicant asserts on page 11, lines 13-16 that the "i" represents unique testing task signals.

Accordingly, withdrawal of the 35 U.S.C. §112, second paragraph, rejections for claims 1-20 are respectfully requested.

II. 35 U.S.C. § 103(a)

It is asserted in the Office Action that claims 1-20 are rejected in the Office Action under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent No. 6,181,151 B1, issued to Wasson ("Wasson"). Applicant respectfully disagrees.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)) Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of " [a]n integrated circuit comprising: a test controller having an instruction register and a test access port finite state machine (TAP FSM); at least one logic unit controller; a test bus directly coupled between the test controller and the at least one logic unit controller; at least one design-for-test-feature coupled to the at least one logic unit controller; and a logic unit coupled to the at least design-for-test-feature wherein said test controller encodes and transmits states of said TAP FSM and test instructions to said at least one logic unit controller over said test bus to test said integrated circuit."

Applicant's amended claim 10 contains the limitations of " [a] platform comprising: an external device; a support structure; a controller disposed on the support structure and coupled to the input device; at least one memory chip disposed on the support structure and coupled to the controller through a processor bus; and an

integrated circuit having a test controller having an instruction register and a test access port finite state machine (TAP FSM), at least one logic unit controller, a test bus directly coupled between the test controller and the at least one logic unit controller, at least one design-for-test-feature coupled to the logic unit controller, and a logic unit coupled to the at least one design-for-test-feature wherein said test controller encodes and transmits states of said TAP FSM and test instructions to said at least one logic unit controller over said test bus to test said platform."

Applicant's amended claim 18 contains the limitations of "... generating a test information packet in a test controller of an integrated circuit; transmitting the test information packet to at least one logic unit controller over a test bus directly coupled between the test controller and the at least one logic unit controller; processing the test information packet within the at least one logic unit controller to generate at least one test control signal; transmitting the at least one test control signal to the at least one design-for-test-feature coupled to the logic unit controller, and testing said integrated circuit."

Applicant's claimed invention tests and debugs an integrated circuit where the integrated circuit contains all necessary components for carrying out the testing or debugging. The distributed test control scheme reduces the number of global test control lines, relaxes routing constraints on the test control lines, and adds greater flexibility in the physical placement of the test controller and test control logic.

Wasson discloses an integrated circuit (IC) tester. Wasson does not disclose, teach or suggest the IC tester is such that it is embedded on the IC to be tested. The IC tester of Wasson is simply external to any IC to be tested. Moreover, Wasson does not teach, disclose or suggest all the limitations contained in Applicant's amended claims 1, 10 and 18, as listed above.

Since Wasson does not disclose, teach or suggest all the limitations contained in Applicant's amended claims 1, 10 and 18, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 1, 10 and 18 are not obvious over Wasson since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly

depend from claims 1, 10 and 18, namely claims 2-9, 11-17, and 19-20, respectively, would also not be obvious over Wasson for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §103(a) rejections for claims 1-20 is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1- 20, patentably defines the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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Dated: June 9, 2003

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Non-Fee Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450 on June 9, 2003.

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Margaux Rodriguez *June 9, 2003*